

Design of Low-Power Coarse-Grained Reconfigurable Architectures

Yoonjin Kim
Rabi N. Mahapatra



CRC Press
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Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism

**Soumitra Kumar Nandy, Masahiro
Fujita**



Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism:

Coarse Grain Reconfigurable Architectures Soumitra Kumar Nandy,Masahiro Fujita,2015-01-29 This book discusses in detail the issues relating to both hardware and software design of coarse grain reconfigurable architectures which can deliver high performance with less energy consumption as the hardware adjusts dynamically for the given application Techniques are described with which the micro architecture can be re structured at the level of groups of operations instead of individual operations as in fine grain reconfiguration Using embedded applications with high performance demands as motivation the book takes the reader step by step through state of the art approaches from defining the architecture to designing execution driven optimizations to realization of the architecture on silicon Empirical results are shown for various real applications *Fine- and Coarse-Grain Reconfigurable Computing* Stamatis Vassiliadis,Dimitrios Soudris,2008-08-12

Compiling for Coarse-grain Reconfigurable Architectures Moshe Morris Emanuel Matsa,1997 **Dynamic Coarse Grained Reconfigurable Architectures** Basher Shehan,2010 Design of Low-Power Coarse-Grained Reconfigurable Architectures Yoonjin Kim,Rabi N. Mahapatra,2010-12-09 Coarse grained reconfigurable architecture CGRA has emerged as a solution for flexible application specific optimization of embedded systems Helping you understand the issues involved in designing and constructing embedded systems *Design of Low Power Coarse Grained Reconfigurable Architectures* offers new frameworks for optimizing the architect **Programming of Coarse-Grained Reconfigurable Architectures** Zain Ul-Abdin,2011 Blocks, Towards Energy-efficient, Coarse-grained Reconfigurable Architectures Mark Wijtvliet,Henk Corporaal,Akash Kumar,2022 This book describes a new coarse grained reconfigurable architecture CGRA called Blocks and puts it in the context of computer architectures and in particular of other CGRAs The book starts with an extensive evaluation of historic and existing CGRAs and their strengths and weaknesses This also leads to a better understanding and new definition of what distinguishes CGRAs from other architectural approaches The authors introduce Blocks as unique due to its separate programmable control and data paths allowing light weight instruction decode units to be arbitrarily connected to one or more functional units FUs over a statically configured interconnect The discussion includes an explanation of how to model architectures resulting in an area and energy model for Blocks The accuracy of this model is evaluated against fully implemented architectures showing that although it is three orders of magnitude faster than synthesis the error margin is very acceptable The book concludes with a case study on a real System on Chip including a RISC architecture the Blocks CGRA and peripherals Provides a comprehensive overview of many coarse grained reconfigurable architectures CGRAs proposed in the last 25 years as well as a classification of those CGRAs Offers a new view on the positioning of CGRAs Provides an in depth description of structure of the Blocks CGRA and its unique aspects Includes an extensive evaluation of various performance aspects of Blocks such as performance energy and area as well as a comparison with various traditional approaches Uses a case study showing how Blocks can be used in a real system on chip and how

performance of this system on chip can be estimated using the proposed model

Fault-tolerant Techniques for Coarse Grained Reconfigurable Architectures, 2010

Compiling Parallel Applications to Coarse-grained Reconfigurable Architectures Mohammed Ashraful Alam Tuhin, 2007

Coarse-grain Reconfigurable Computing Ethan Avram Mirsky, 1996

New Algorithms, Architectures and Applications for Reconfigurable Computing Patrick Lysaght, Wolfgang Rosenstiel, 2005-12-05

New Algorithms Architectures and Applications for Reconfigurable Computing consists of a collection of contributions from the authors of some of the best papers from the Field Programmable Logic conference FPL 03 and the Design and Test Europe conference DATE 03 In all seventy nine authors from research teams from all over the world were invited to present their latest research in the extended format permitted by this special volume The result is a valuable book that is a unique record of the state of the art in research into field programmable logic and reconfigurable computing The contributions are organized into twenty four chapters and are grouped into three main categories architectures tools and applications Within these three broad areas the most strongly represented themes are coarse grained architectures dynamically reconfigurable and multi context architectures tools for coarse grained and reconfigurable architectures networking security and encryption applications Field programmable logic and reconfigurable computing are exciting research disciplines that span the traditional boundaries of electronic engineering and computer science When the skills of both research communities are combined to address the challenges of a single research discipline they serve as a catalyst for innovative research The work reported in the chapters of this book captures that spirit of that innovation

Designing Cost-effective Coarse-grained Reconfigurable Architecture Yoonjin Kim, 2010

Application specific optimization of embedded systems becomes inevitable to satisfy the market demand for designers to meet tighter constraints on cost performance and power On the other hand the flexibility of a system is also important to accommodate the short time to market requirements for embedded systems To compromise these incompatible demands coarse grained reconfigurable architecture CGRA has emerged as a suitable solution A typical CGRA requires many processing elements PEs and a configuration cache for reconfiguration of its PE array However such a structure consumes significant area and power Therefore designing cost effective CGRA has been a serious concern for reliability of CGRA based embedded systems As an effort to provide such cost effective design the first half of this work focuses on reducing power in the configuration cache For power saving in the configuration cache a low power reconfiguration technique is presented based on reusable context pipelining achieved by merging the concept of context reuse into context pipelining In addition we propose dynamic context compression capable of supporting only required bits of the context words set to enable and the redundant bits set to disable Finally we provide dynamic context management capable of reducing reduce power consumption in configuration cache by controlling a read write operation of the redundant context words In the second part of this dissertation we focus on designing a cost effective PE array to reduce area and power For area and power saving in a PE array we devise a costeffective array fabric addresses

novel rearrangement of processing elements and their interconnection designs to reduce area and power consumption In addition hierarchical reconfigurable computing arrays are proposed consisting of two reconfigurable computing blocks with two types of communication structure together The two computing blocks have shared critical resources and such a sharing structure provides efficient communication interface between them with reducing overall area Based on the proposed design approaches a CGRA combining the multiple design schemes is shown to verify the synergy effect of the integrated approach Experimental results show that the integrated approach reduces area by 23.07% and power by up to 72% when compared with the conventional CGRA

Programming Fine-grained Reconfigurable Architectures Steven Anthony

Guccione,1995 Recently several systems based on reconfigurable logic have been designed and built These systems permit arbitrary digital logic functions to be configured in hardware This ability to dynamically configure such circuits promises to provide the flexibility of a software based system with the performance of custom hardware This dissertation proposes a high level language approach to programming reconfigurable logic based machines This approach uses a data parallel variant of the C language To support this high level language approach a novel reconfigurable logic device is described These devices are in turn interfaced to a memory system and used to perform computation To demonstrate the validity of this approach several computationally intensive algorithms are implemented and simulated Among these algorithms are cellular automata image processing neural networks the Mandelbrot set and the Fourier transform In addition selected portions of the Livermore FORTRAN kernels are simulated Estimates of performance and required system resources are reported for each algorithm

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1. Understanding the eBook Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - The Rise of Digital Reading Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Advantages of eBooks Over Traditional Books
2. Identifying Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - User-Friendly Interface
4. Exploring eBook Recommendations from Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Personalized Recommendations
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism User Reviews and Ratings

- Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism and Bestseller Lists
- 5. Accessing Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism Free and Paid eBooks
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism Public Domain eBooks
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism eBook Subscription Services
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism Budget-Friendly Options
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 - ePub, PDF, MOBI, and More
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism Compatibility with Devices
 - Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Highlighting and Note-Taking Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Interactive Elements Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
- 8. Staying Engaged with Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
- 9. Balancing eBooks and Physical Books Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Setting Reading Goals Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Fact-Checking eBook Content of Ebook Online Coarse Grain Reconfigurable Architectures Polymorphism
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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